CONTINUOUS FREQUENCY COVERAGE AND RANGE EXPANSION IN PLL-BASED FREQUENCY SYNTHESIZERS

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Abstract: *This paper analyzes methods for expanding the synthesized frequency range in phase-locked loop (PLL)-based frequency synthesizers with an emphasis on achieving continuous frequency coverage. The study examines 3 based on integer frequency relationships using frequency division and multiplication within a single PLL loop. A condition for continuous frequency coverage is formulated, ensuring overlap between adjacent synthesis configurations and preventing frequency gaps. The influence of frequency division coefficients, harmonic selection, and conversion stages on spectral purity and phase noise performance is discussed. A circuit architecture employing a low-noise high-frequency reference oscillator and commercially available PLL integrated circuits is considered. The analysis demonstrates that wideband frequency synthesis with high spectral quality can be achieved while limiting the number of frequency conversions and maintaining structural simplicity. The obtained results provide practical guidelines for the design and optimization of wideband frequency synthesizers requiring stable operation and continuous tuning.*

Keywords: *phase-locked loop (PLL), frequency synthesizer, wideband frequency synthesis, continuous frequency coverage, frequency division and multiplication, phase noise, spectral purity.*

In the design of frequency synthesizers, it is necessary to take into account a number of associated technical challenges. In particular, the presence of auxiliary signal sources operating at different frequencies has a significant impact on the overall system performance. Under such conditions, ensuring proper signal matching and interconnection at frequency conversion and processing nodes becomes critically important. Improper coupling may lead to spectral contamination, the appearance of spurious sidebands, and an increase in the overall noise level. In addition to the considered circuit configuration, frequency synthesizers capable of generating a fine frequency grid with comparable performance characteristics can be implemented using various structural approaches. In particular, modifying interconnection scheme of standard integrated circuits, combining certain functional blocks, or achieving more efficient utilization of components allows a reduction in overall circuit complexity. Such an approach not only optimizes hardware resources but also improves the energy efficiency of the system [1]. For example, when additional circuit blocks

implementing frequency division with a factor of $N_3 = 123$ were incorporated into the synthesizer architecture, the spectral characteristics of the output signal were analyzed using a spectrum analyzer. The obtained results showed that the highly suppressed auxiliary spectral components remained within the specified permissible limits, confirming the practical feasibility and effectiveness of the selected structural solution [1, 2].

At the same time, during the formation of the frequency grid, the involvement of auxiliary devices and multiple signal sources necessitates frequent processing and transmission of signals with varying frequencies. This circumstance highlights the importance of carefully selecting frequency conversion nodes and interconnection points in the synthesizer design. To address these challenges, the use of standard microelectronic components, adaptation of their interconnection schemes, and the introduction of alternative structural modifications can be considered as effective design solutions. Let us now consider an example of signal generation over a wide frequency range (Fig.1). In the presented circuit, an additional element is introduced, denoted as C, which represents a frequency multiplier [3].

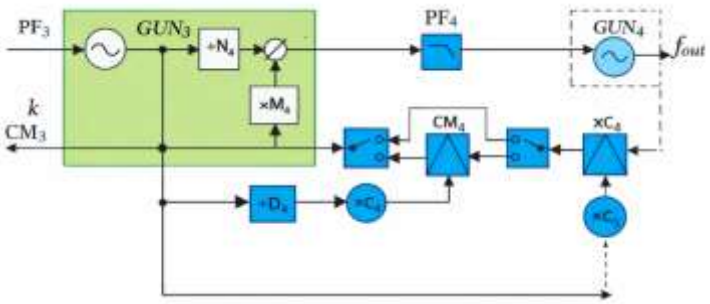

Figure 1. Expansion of the synthesized frequency range.

The given configuration can be regarded as a continuation of the fine-step frequency synthesizer, where it operates as a tunable reference signal source. In this scheme, the concept of multiple frequency conversions within a single PLL loop is implemented [1, 6, 8], while maintaining integer frequency relationships among the frequencies involved in the synthesis process. From a design perspective, it is desirable to minimize the number of frequency conversion stages. In the considered case, the number of such conversions is limited to two. As a result, to achieve octave coverage, it becomes necessary to utilize the harmonics of the signal at the output of the frequency divider D4. The required harmonic content strongly depends on the tuning range of the reference signal source [4]. The narrower the tuning range, the larger the division factor of the D4 frequency divider that must be employed. This, in turn, leads to a denser arrangement of harmonics, increased circuit complexity, and may cause an excessive rise in phase noise. In the general case, for each configuration of the frequency range expansion scheme, it is possible to derive an expression that linearly relates the output signal frequency to the input signal frequency, while ensuring compliance with the integer frequency relationships imposed by the PLL-based synthesis process [1, 6, 8].

$$f_{\text{out}}(i, f_3) = k_i \cdot f_3$$

Here, i denotes the index of the synthesizer configuration, corresponding to the ordered set of proportionality coefficients k_i arranged in ascending order. Under this definition, the condition for continuous frequency coverage can be expressed as follows.

$$f_{\text{out}}(i,\ f_{3,\max}) \ \geq \ f_{\text{out}}(i+1,\ f_{3,\min})$$

Figure 2 presents a graphical interpretation of this expression. The requirement to maintain integer frequency relationships implies that the frequency division factor N4 can take only a limited set of discrete values, namely those cases in which the values of N4 are integer multiples of the frequency division factor D4. In this scheme, particular attention must also be paid to ensuring proper interconnection and isolation between functional blocks, especially in order to prevent interference originating from auxiliary signals from propagating to the output. Such interference may result in the appearance of unwanted spectral components and an increase in the phase noise level of the output signal [4, 5].

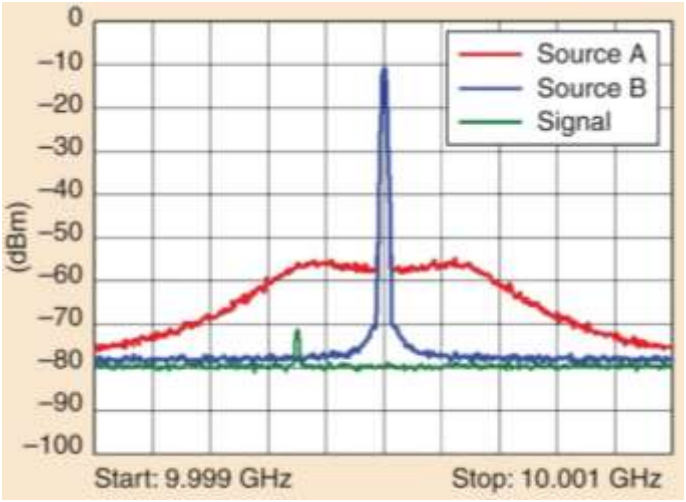

Figure 2. Condition for continuous frequency coverage.

Therefore, during the circuit design process, special consideration should be given to filtering, shielding, and the separation of signal paths. Moreover, due to the requirement to maintain integer frequency relationships, the frequency division factor N4 can assume only a limited and discrete set of values. Although this constraint reduces the tuning flexibility of the synthesizer, it plays a crucial role in ensuring the spectral purity and stability of the output signal. The considered circuit solution demonstrates the feasibility of achieving high-quality signal spectra over a wide frequency range [6, 7]. In this approach, a low-noise high-frequency generator is employed as the reference signal source, while commercially available PLL integrated circuits are used as the synthesis elements. This design strategy enables stable operation and high spectral performance without a significant increase in hardware complexity.

Conclusion. In this work, the problem of synthesized frequency range expansion in PLL-based frequency synthesizers has been analyzed. It has been shown that, although the tuning range of individual synthesis stages is limited, continuous frequency coverage can be achieved by properly selecting frequency division and multiplication coefficients while maintaining integer frequency relationships. The derived condition for continuous frequency coverage provides a clear criterion for avoiding frequency gaps between adjacent synthesis configurations. The analyzed circuit architecture demonstrates that wideband frequency synthesis with high spectral quality can be realized using a low-noise reference oscillator and standard PLL integrated circuits, without excessive structural complexity. The presented results confirm that the proposed approach is well suited for practical applications requiring stable, wideband, and spectrally pure frequency generation.

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